PFC CCM with XMC

XMC1000 & XMC4000

About this document

Scope and purpose

This document presents the concept and implementation of a Power Factor Correction (PFC) Continuous Conduction Mode (CCM) with XMC. The document describes as well how to address specific operation points where DCM mode is required.

Althougt the concept and code can be applied to several XMC products the practical implementation has been carried out on **EVAL_800W_130PFC_C7** PFC Platinum server board having a XMC1300 or XMC1400 as controller.

Intended audience

The target audience of this document is any technical person interested in the development or adaptation of Infieon PFC CCM code example.

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1 PFC CCM introduction

1.1 Overview

Power Factor Correction (PFC) shapes the input current of the power supply to maximize the real power taken from the line by shaping the current and keeping it in phase respect to the input voltage. In an ideal PFC circuit, the input current follows the input voltage as a pure resistor, consuming no apparent power.

1.2 Topology

Although active PFC can be achieved by several topologies, the boost converter (Figure 1) is one of the the most used topology due to its simplicity.

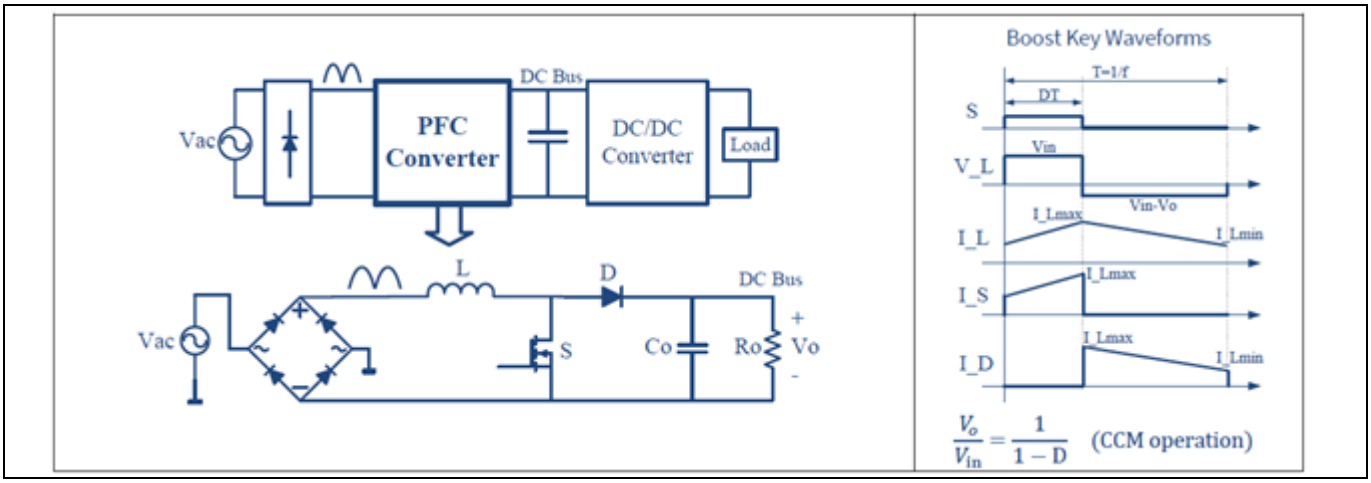

Figure 1 PFC boost topology

1.3 PFC operation modes

The boost converter can operate in three modes: continuous conduction mode (CCM), discontinuous conduction mode (DCM), and critical conduction mode (CrCM). Figure 2 shows modeled waveforms to illustrate the inductor and input currents in the three operating modes, for the same exact voltage and power conditions.

In general the operation mode is driven by the power range to be delivered; tipically CCM is used for higher power ranges than DCM or CrCM.

CCM operation operation can be achieved with constant or variable switching frequency, although normally constant frequency operation simplifies the input filter design.

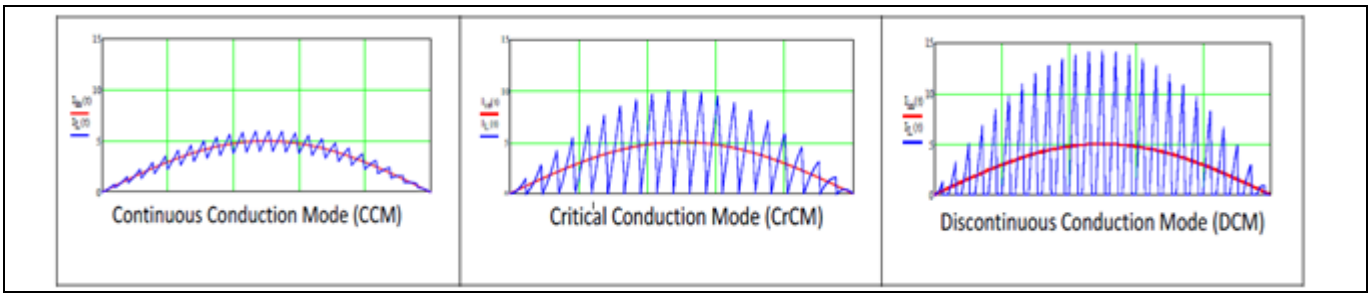

Figure 2 PFC operation modes

CrCM may be considered a special case of DCM, where the operation is controlled to stay at the boundary between CCM and DCM, for that an additional input for zero crossing detection is used. If only CrCM operation is used, constant on-time control can be used resulting in variable frequency.

For fix switching frequency operation, the input voltage and power output of the PFC will determinate the operation mode, in this way we may have:

- Complete half AC cycle in CCM operation mode
- Complete half AC cycle in DCM operation mode
- DCM and CCM operation modes during half AC cycle

The boundaries between such operation modes can be calculated theoretically, an example is shown in Figure 3:

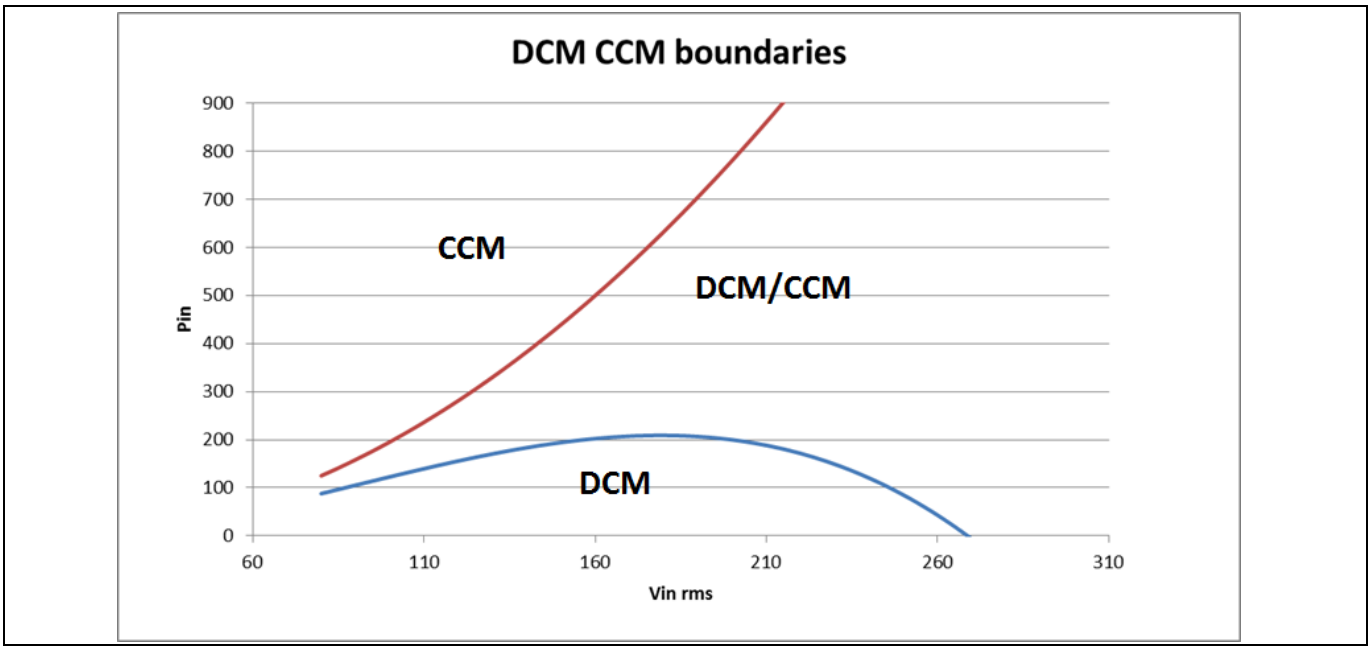

Figure 3 Operation mode boundaries

In this document we will focus on a constant frequency PFC due to its advantage of simplified imput filter and solve the different operation modes with the XMC digital controller to maximize the performance of the whole system. The proposed concept and implementation will cover DCM and CCM operation mode, therefore we can say that the algorithm supports multimode operation.

2 Regulation algorithms

The output of the porposed PFC is regulated in voltage; therefore we will need a voltage feedback and the corresponding regulation loop to keep constant DC average value at the output.

Due to the used topology and the need for power factor and low input current THD, the output will contain a considerable ripple added to the DC output voltage which depends on the load conditions, due to that special care for output voltage sensing needs to be taken.

In other hand we will need to provide a current that follows in a proportional manner the input voltage to keep good power factor and input current THD.

To solve the previous mentioned challenges a feedback loop topology will be used, with a voltage loop controlling an inner current loop.

2.1 Voltage control loop

Load model: if we assume small variation of the output voltage (normally the case due to the big output capacitor), we can see our system as a current source feeding the output capacitor and we can represent the PFC load as a current sink taking energy from our output capacitor.

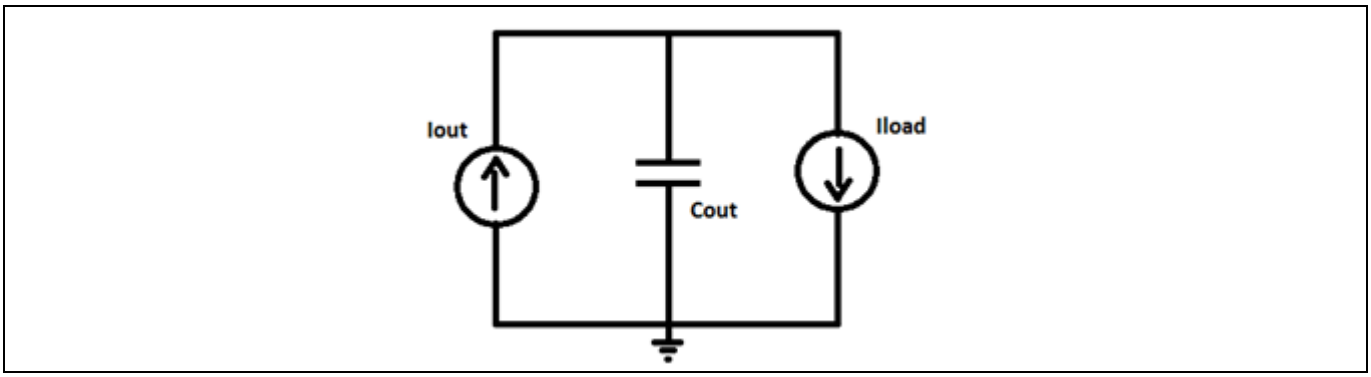

Figure 4 Simplified PFC plant

The resulting voltage loop with its inner current block is presented in Figure 5.

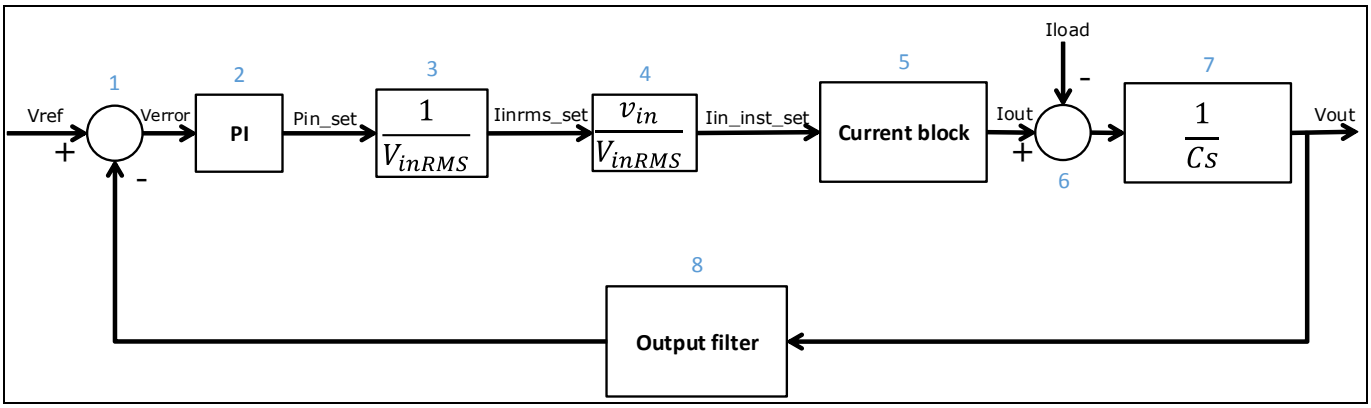

Figure 5 Voltage loop block diagram

The different blocks of the voltage loop are described in Table 1.

Table 1 Voltage loop blocks

Block number	description
1	Subtraction to calculate the error from the reference voltage
2	PI regulator
3	Input current RMS calculation
4	Current shaping according to input voltage
5	Current block, ensure that input current follow the instantaneous given value
6	Total current flowing into the output capacitor
7	Output capacitor model
8	Filter used to extract the DC value from the output voltage

From this diagram we can give units to the **P** and **I** part of our **PI** regulator:

- **P** will be measured in Watts/volt.
- **I** will be measured Watts/(volts*s)

Special attention we have to put in the output voltage filter, a low pass filter would add a delay into our system that may result into instable loop or slow regulation. To avoid such issue an optional notch filter plus a non lineal filter are suggested.

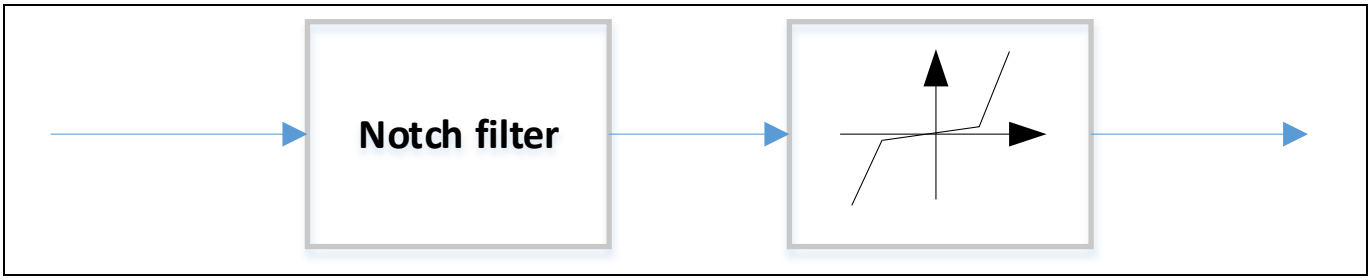

Figure 6 Output filter

The notch filter would reject the major frequency of the output voltage (100Hz or 120Hz); a selection is done during start up depending of the line frequency.

The non lineal filter ensures a smooth response for small drifts of the output voltage but increase its response when the output drift is too high to ensure a good response during load or line transients.

2.2 Current control loop

The current loop will ensure that a given current is sunk from the line, indepent on the load and line conditions. As can be seen in Figure 3 the required operation mode may change and results into only CCM mode, only DCM mode or a mix which change along half AC cycle.

To find out the operation mode boundary let´s look at the inductor current shape. The border between CCM and DCM ocurrs when the lower value of the current hits zero at the end of the off phase, in other words, the peak to peak current is double than the average current.

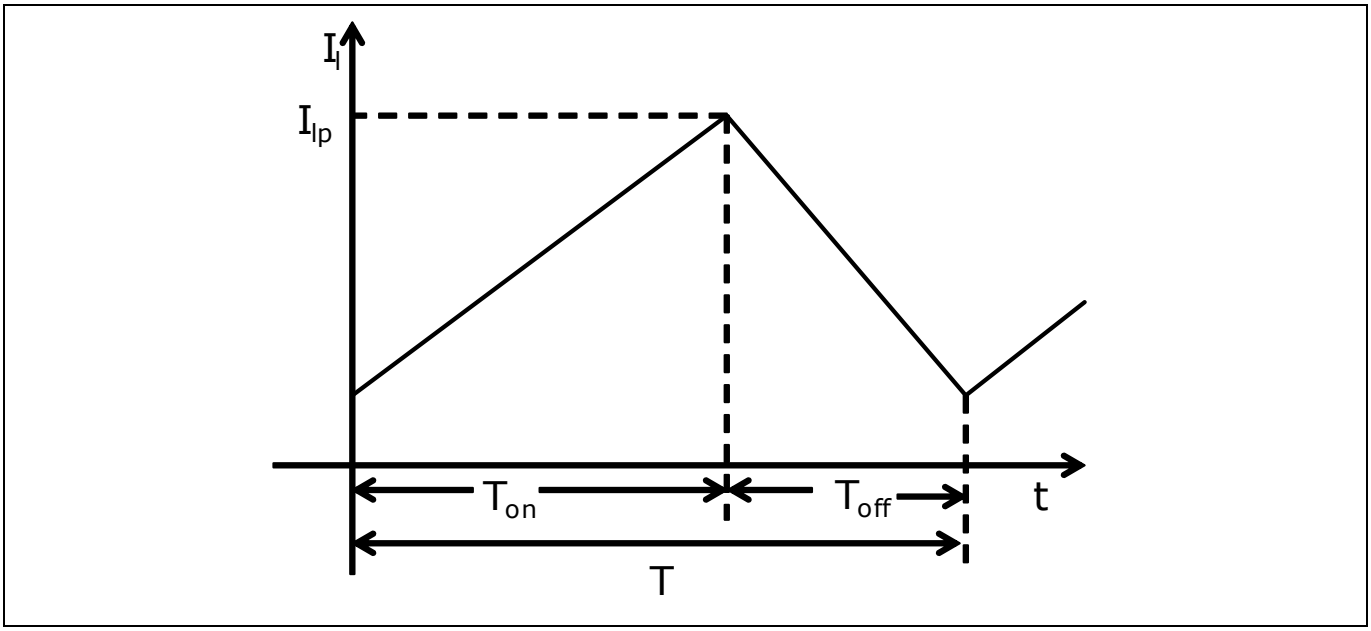

Figure 7 Inductor current shape during CCM operation

Assuming the switching frequency is high compare to the frequency line, we can say that the the base duty cycle in CCM (D_{Bccm}) is:

$$[1] \quad V_{in}T_{on} = (V_{out} - V_{in})T_{off}$$

$$[2] \quad D_{Bccm} = 1 - \frac{V_{in}}{V_{out}}$$

From Figure 7 we can say that the inductor peak to peak current is:

$$[3] \quad I_{lpp} = \frac{V_{in}}{L}T_{on}$$

The condition to have DCM is that $I_{lpp}>2I_{set}$, where I_{set} is the desired average current, considering that and the previous equations we have the condition for DCM is:

$$[4] \quad V_{in}D_{Bccm} > 2\frac{L}{T}I_{set}$$

We can use the previous equation to evaluate when DCM operation occurs either during a complete or partial half cycle.

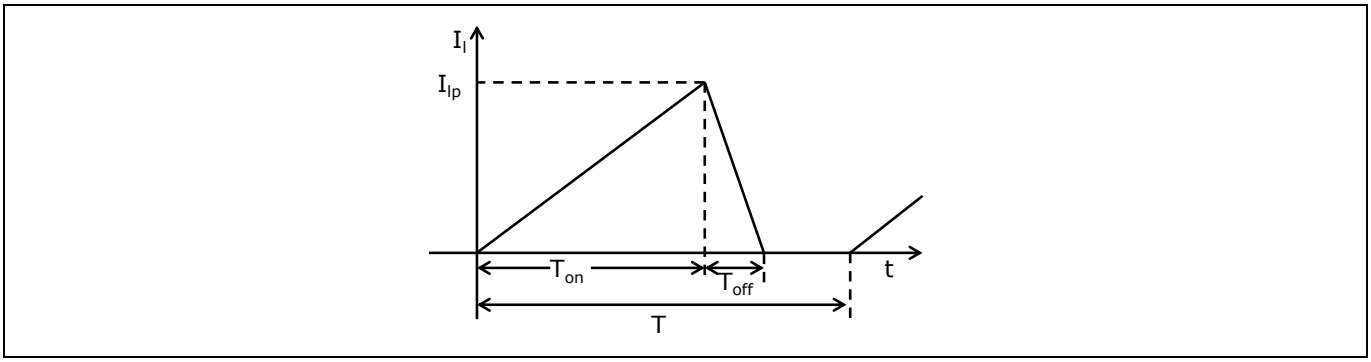

Figure 8 Inductor current shape during DCM operation

During DCM operation the base duty cycle required comes from the equation [6]:

$$[5] \quad I_{Lpeak} = \frac{V_{in}T_{on}}{L} = 2I_{set}\frac{T}{T_{on}+T_{off}}$$

$$[6] \quad D_{Bdcm} = \sqrt{\frac{2LI_{set}D_{Base}}{TV_{in}}}$$

Looking at the gains in steady state for CCM and DCM we have as well two different equations:

$$[7] \quad \text{For CCM: } \frac{dI}{dD} = \frac{TV_{out}}{L}$$

$$[8] \quad \text{For DCM: } \frac{dI}{dD} = \frac{V_{in}TD_{Bdcm}}{LD_{Bccm}}$$

The gain shown for DCM and CCM are different and normally there is an abrupt change of gain at the boundary.

In Figure 9 we can see the operation mode for the next conditions (considering no losses):

- Switching frequency: 128KHz
- Inductance value: 210µH
- Vac RMS: 230V
- Input current: 1A
- Output voltage: 380V

Figure 10 shows the change of the gain due to the different operation modes for the same condtions.

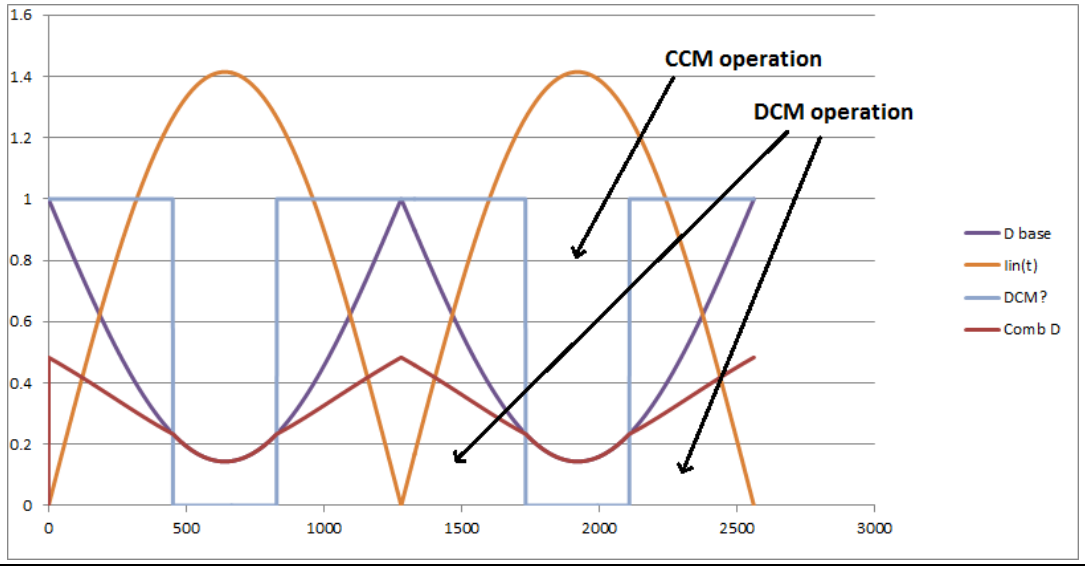

Figure 9 Operation mode over half AC cycle

Figure 9 shows the CCM base duty cycle (D_{Bccm}, D_{base}) calculated previously and the required duty cycle required for DCM operation. The combination of both results in Comb D, from that we can say that a pure CCM algorithm would not ensure good current shape under all conditions.

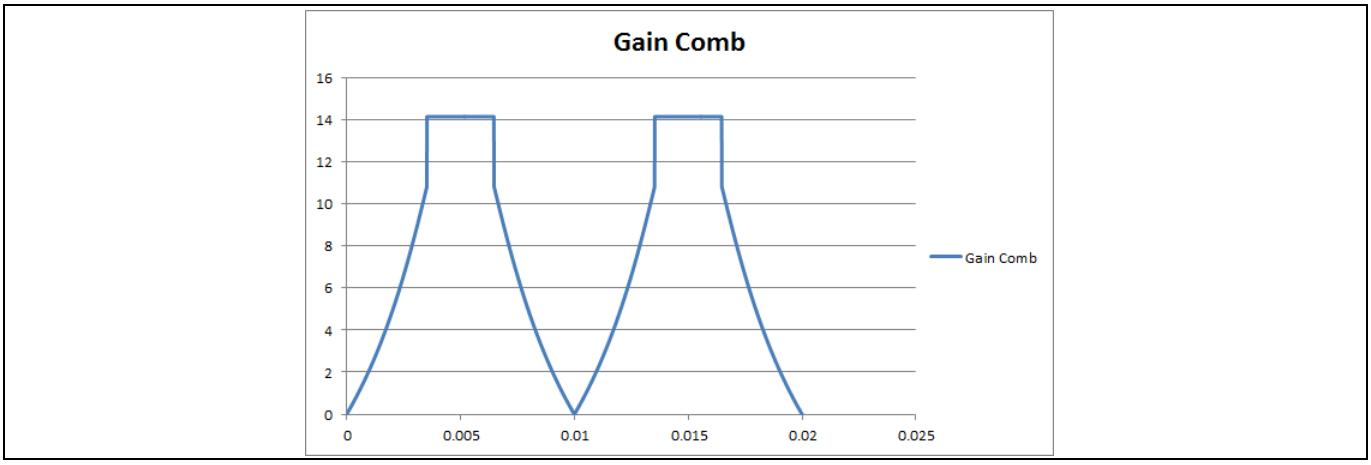

Figure 10 Plant gain over one AC cycle

The used algorithm will add to the current PI output the required base duty cyle to reduce the effort of the PI to follow the current, at the same time the proportional part can be modify to linearize the system in such way that there is no need for PI trimming depending on load and line conditions, reducing the effort for adapting the code to a new design.

Additional aspects to consider are:

- Distiguish when we have CCM or DCM mode
- In DCM calculate the real average current compare to the measured current.
- Change the proportional part of the PI according to the plant DCM or CCM

Since the plant gain in DCM is normally less and in some cases much less than the gain in CCM, the proportional part of the PI has to be higher for DCM than CCM. Correcting for such gain change brings the risk of having CCM operation with the required compensator gain of DCM which would result in a current overshoot and/or oscillations. Therefore appropriate measured has to be taken to avoid such situation.

Three factors are introduced to avoid such situation:

- The operation mode assumed is the one which gives the minimum duty cycle
- The used CCM duty base is multiplied by a constant less than 1 to ensure an early entry and late exit in CCM mode.
- The compensator gain used for CCM (less than DCM gain) is used in DCM around the boundaries.

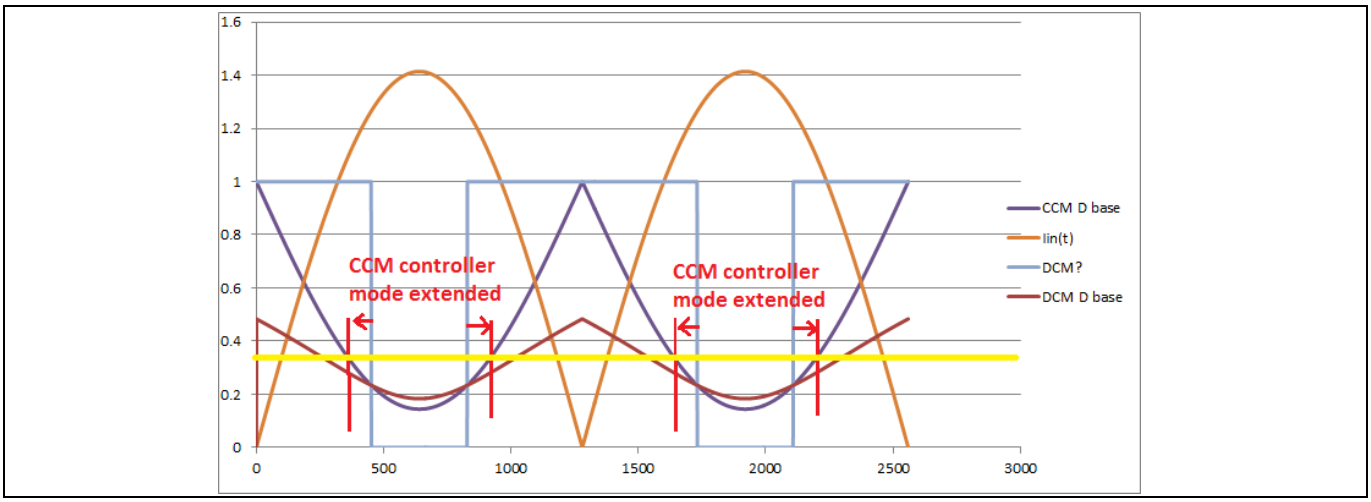

Figure 11 Controller proportional gain change

In particular the gain is changed when the DCM duty base is bellow CCM duty base plus a given delta.

The correction of the measured average current respect to the sampled one is a function of the duty base for DCM and CCM as shown in equation [9].

$$[9] \quad I_{avg} = I_{sam} \frac{D_{Bdcm}}{D_{Bccm}}$$

Considering everthing the algoritm can be sumarize in Figure 12:

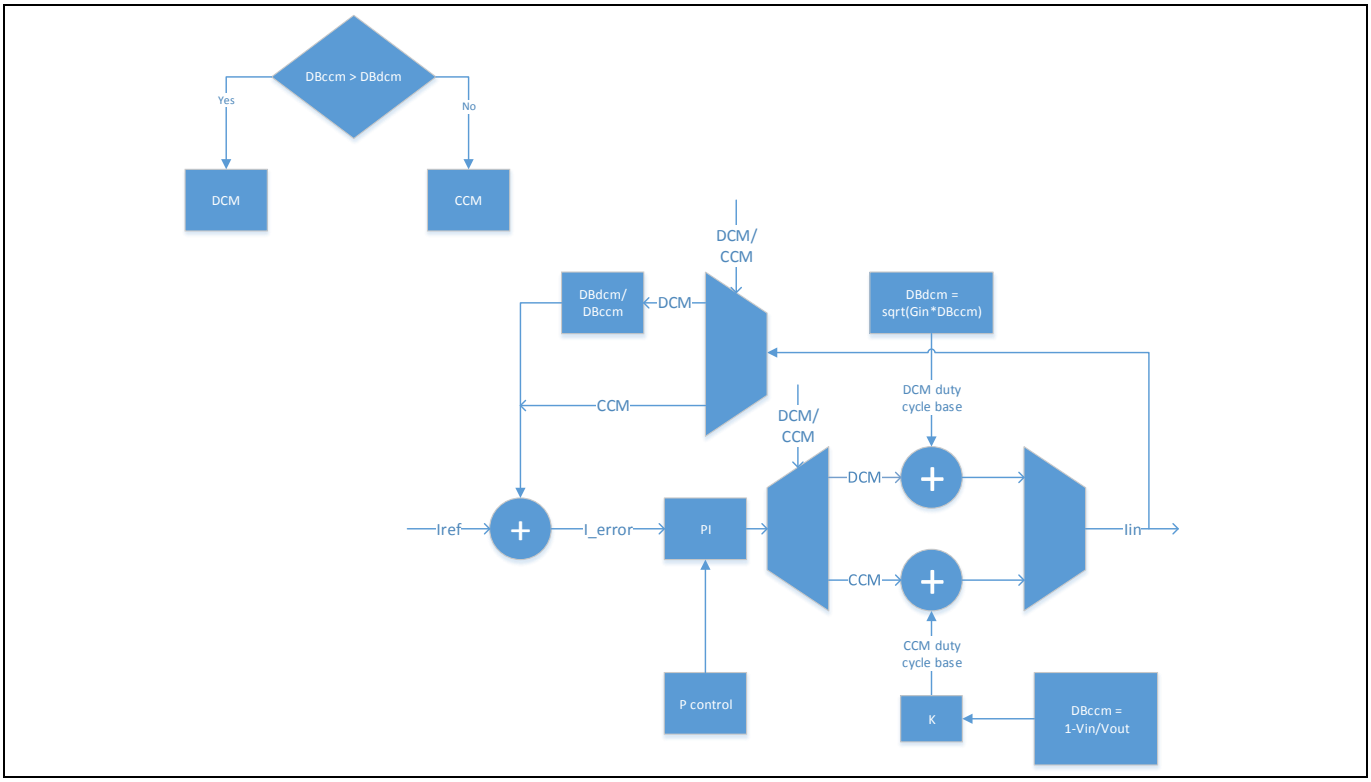

Figure 12 Current loop block diagram

2.2.1 Practical improvements to the current loop

The performace in terms of input current THD could be further improved by enforcing certain operation mode under certain load and line conditions, for example, when only a small portion of the half AC wave requires DCM operation, it is better to use only the CCM algorithm because it will result in a smoother current shape. This is not implemented in the current version

2.2.2 Additional considerations for the current loop

Different effects need to be taken into account to ensure a full performance of the system.

- Compensator proportional part adjustment
- Mosfet output capacitor effect

The compensator proportional part is adjusted upon the operation mode as explained in chapter 2.2, and additionally, the compensator gain for every mode includes the inverse of the plant gain multiplied by a constant in order to linearize the plant behavior, see equations [10] and [11].

[10] For CCM: $P = k_{ccm}\frac{L}{TV_{out}}$

[11] For DCM: $P = k_{dcm}\frac{LD_{Bccm}}{V_{in}TD_{Bdcm}}$

Addtionally the variation of the inductance with the current has to be taken into account by decreasing the compensator proportional part as the input current increases.

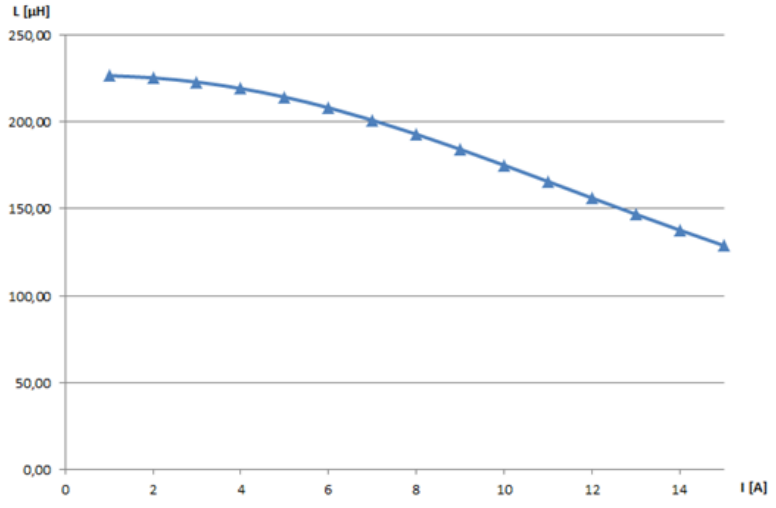

Figure 13 Inductance vs. current dependency

Correcting such variations will avoid oscillations of the input current when its value is too high. The compensation is done assuming a lineal decrease of the inductance with the current.

All corrections of the proportional gain for the current loop are covered in the example code.

The second effect that will corrected is the effect of the mosfet output capacitor. As shown in Figure 14, the current in the inductance (yellow) continue flowing while the output mosfet capacitance is being charged (blue Vds) even if the gate drivers is already off(red) .

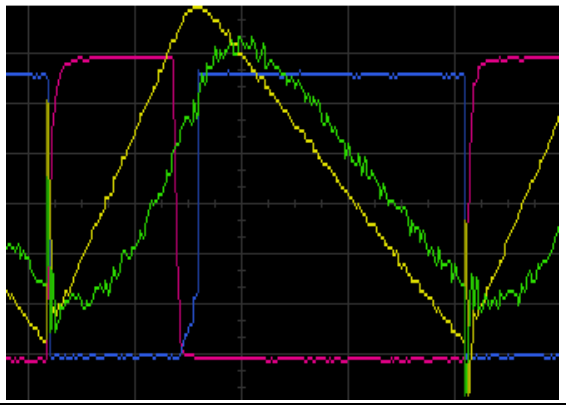

Figure 14 Coss effect on the inductance current

Such effect is visible in the input current shape around the zero crossing for high RMS input current values, under such conditions the duty cycle is almost one and the resulting effect leads to “concatenated-like” pulses until the input current is high enough to bring the Vds up.

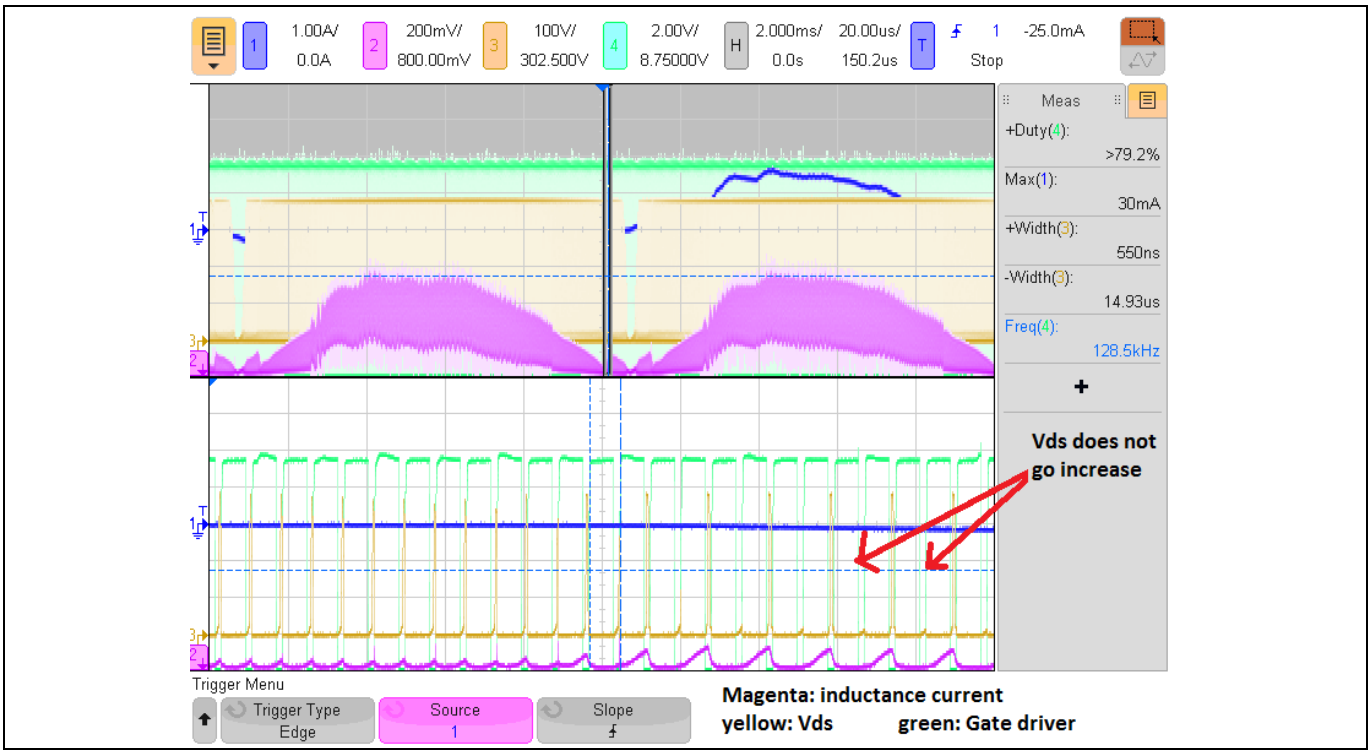

Figure 15 Coss effect on the inductance current

Such correction improves the current shape during zero crossing of the input voltage for high load low line operation, allowing value of THD bellow 2%.

2.3 Other functionalities

2.3.1 Pseudo PLL and RMS calculation

One of the basic variables required for the regulation loops is the input voltage RMS value. To allow a fast reaction it is desired to have the value update as soon as possible. Just think about a line transient where an increase of input voltage does not result into a decrease of the input current. The energy transferred may increase significantly.

Althoug the feedforward used in the current loop for the duty base calculation helps, a pseudo PLL synchronized with the input voltage zero crossing has been implemented. At every voltage zero crossing the average value of the input voltage for the last half AC cycle will be measured. Assuming a perfect rectified sine wave the RMS value is extracted by multiplying the average by a given factor: 1.11 (RMS value/average value).

The PLL has additional functionality such as a counter to measure the input voltage frequency, which will be used to determine the notch filter to be used (100Hz rejection or 120Hz rejection) in case it is not bypass.

2.3.2 Start up phase

The start up phase is the time taken to bring the output voltage into its regulation point, to allow a smooth start up a programmable ramp can be configured in the SW that will result in a progressive increase of

the reference voltage. Such approach helps the user to avoid overshoots and excesive current to charge the output capacitor.

2.4 Limits and protection

Several limits and protection features have been implemented to ensure the safe operation of the whole system; they can be divided into HW protections and SW limits and protections.

2.4.1 HW protections

There are 2 hardware protections implemented with comparators that will deactivate the gate driver in case they are triggered.

- Output overvoltage protection: the comparator is feed with a constant voltage (limit) and the output voltage scaled for comparison.
- Inductor overcurrent protection: the comparator is feed with a constant voltage (limit) and the input current sensed for comparison.

2.4.2 SW limits and protections

While the application is running several limits are applied to avoid stress of the components (limits will not trigger a shut down):

- Instantaneous input current: limit the value of the requested instantaneous current set point for the current loop
- Instantaneous input power: limit the value of the PI output in the voltage loop which represents the transfered power.
- Instantaneous input conductance: limit the value of the set input conductance value (Irms/Vrms).
- Output voltage limit: if the output voltage is over this limit the requested input power of the system is set to 0.
- Duty cycle minimum and maximum values
- Absolute value of the delta duty cycle: limit the change of the duty cycle per update.

Additionally several protections are implemented by SW which leads to system shut down:

- Output voltage protection: if the measured output voltage is over a given protection theshold a shut down will be trigger.
- Input current protection: if the measured input current value is over a given protection threshold a shut down will be trigger. Particularly this proteccion can be defined separately for output voltage ramp up and tracking
- Overload: if the system detects that the average output voltage fall below a given value this protection will be trigger.

3 XMC implementation

In the next chapter we will discuss the implementation example carried out on XMC1300 from SW and HW point of view.

3.1 Software implementation

The software has been structured in different layers to preserve modularity and easy HW access:

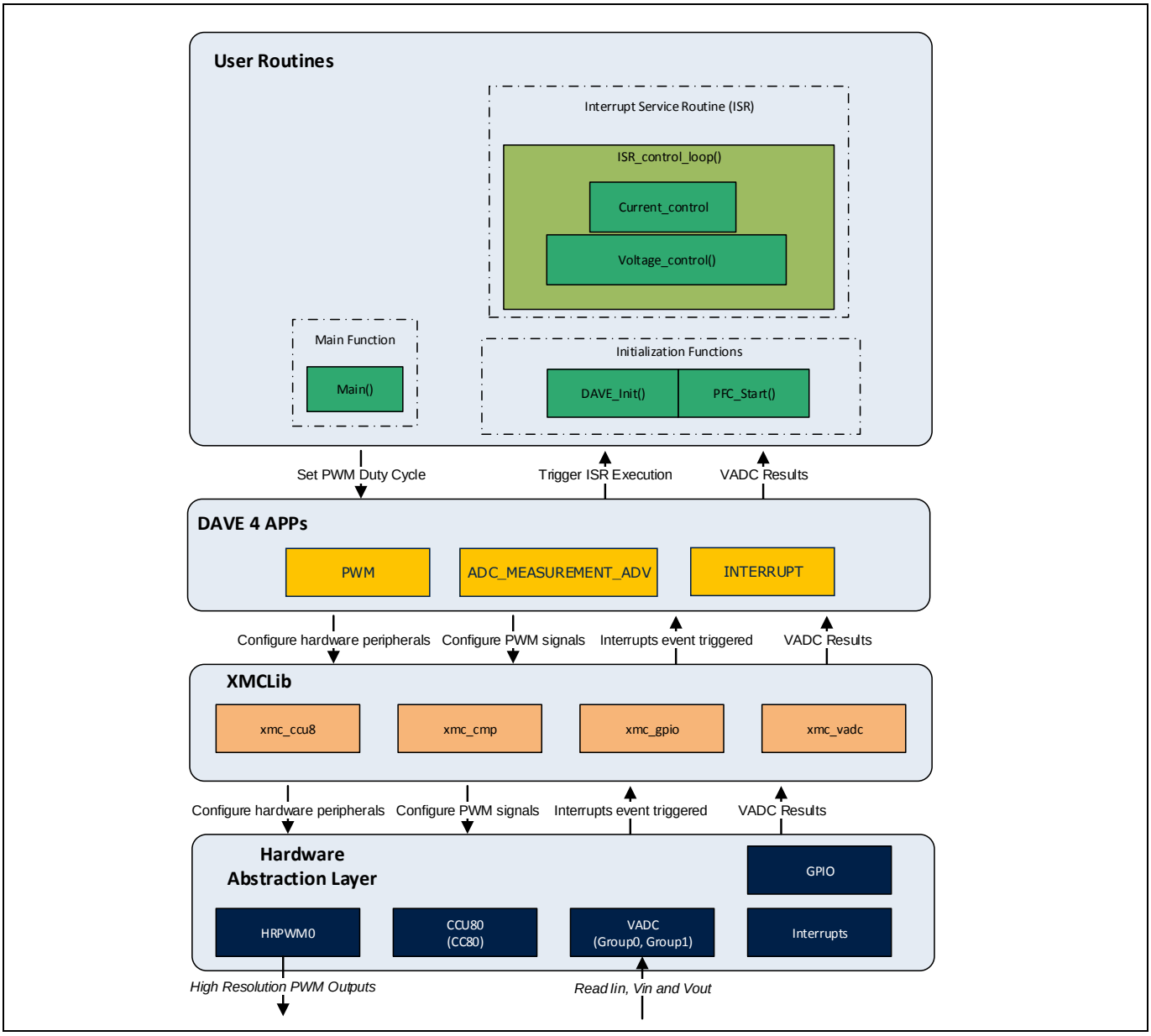

Figure 16 SW layer overview

- The lower level is the hardware access, ie. HW registers definion,
- On top of it XMClib is used, such library implements APIs that simplify the interface to the peripherals
- Dave APPs are used only during initialization and helps the user to easy assign pins and initiaze the peripherals, ie: Vin pin, ADC sampling time, ADC sampling order, etc
- On top the initialization functions and control loop are found, which are of most interest for the final user.

3.2 Harware usage and configuration

The software example used the next peripherals:

- 2 comparators
- 1 Capture and Compare Unit (CCU4)
- 3 ADC channels: Vin, Iin and Vout
- Division unit (part of MATH coprocessor)

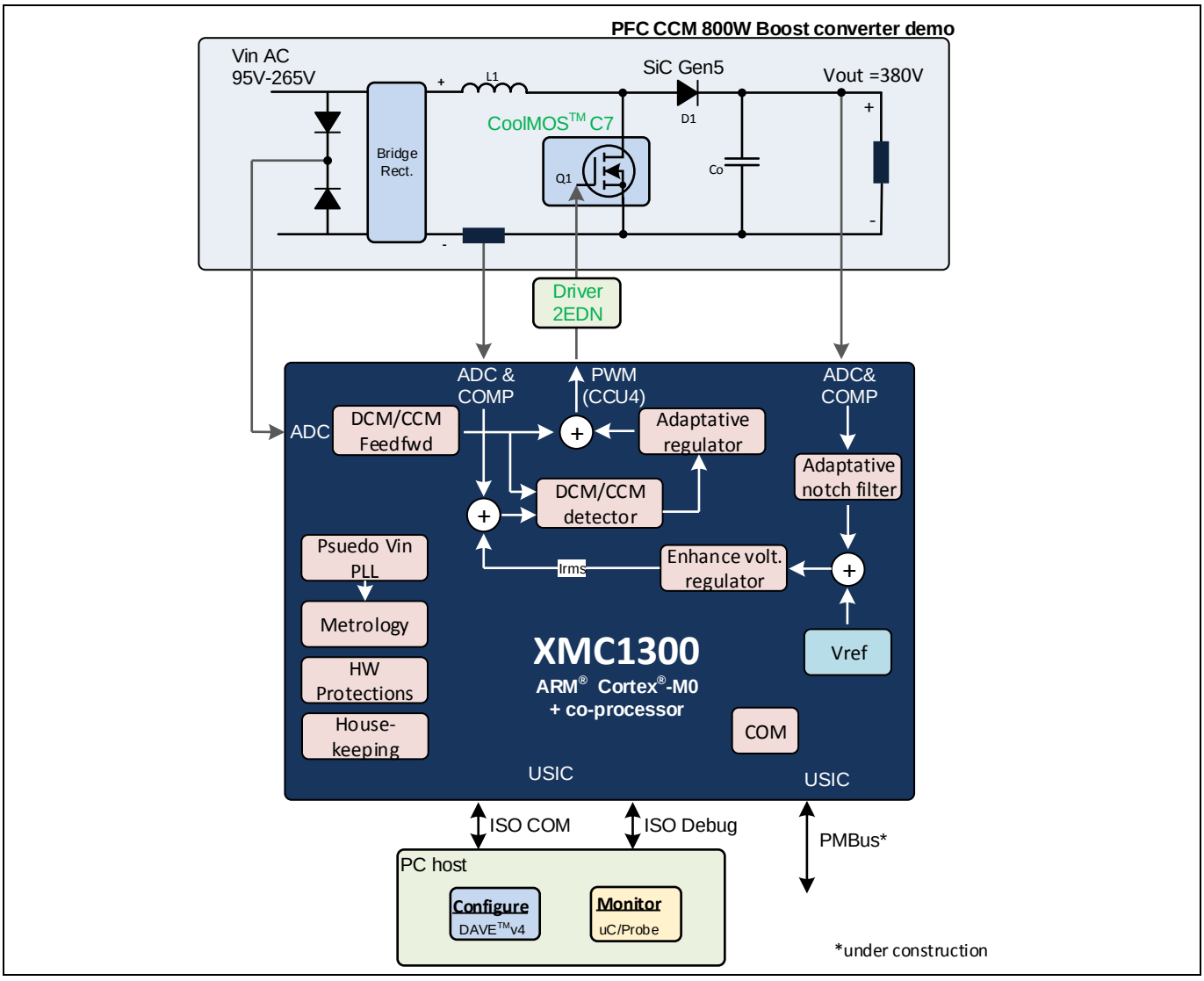

Figure 17 Interface between PFC HW and XMC

The two comparators are used for HW overvoltage and overcurrent protection leading to a switch off of the gate driver when triggered. The software can check if such protection has been trigger by checking the staus of the TRAP funcionality.

The CCU4 unit is used for three porposes:

- Generate the PWM for the gate driver
- Trigger the corresponding ADC conversions synchronized with PWM
- Trigger the interrupt for the control loops

XMC implementation

CCU4 slide 0 is configured in center aligned mode with a compare value that will modulate the gate driver output.

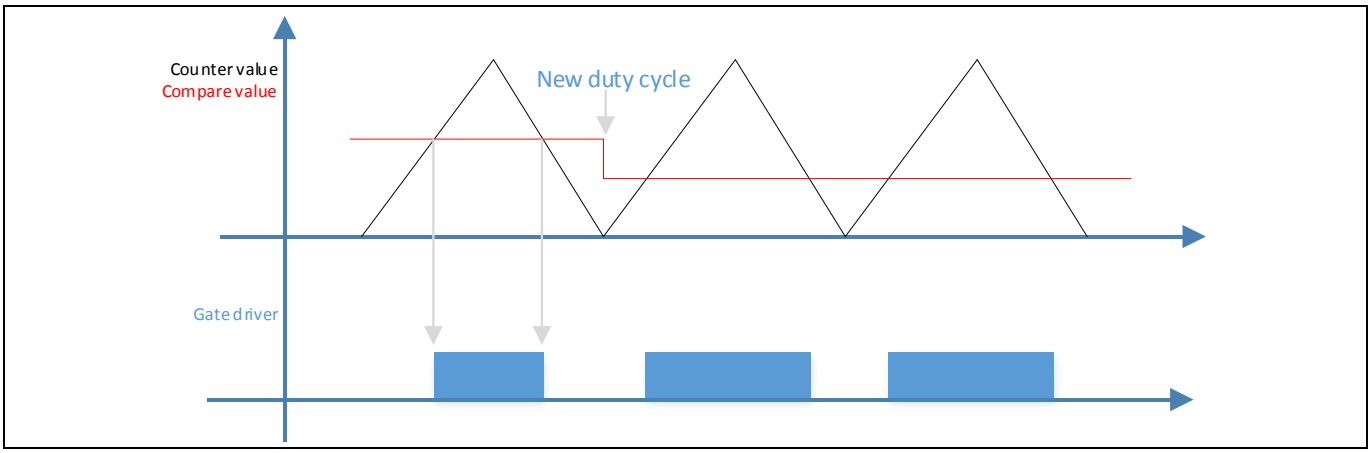

Figure 18 Gate driver modulation with CCU

CCU4 slide 3 is used to trigger an interrupt perdiocally and synchronized with the switching frequency, in particular the the interrupt is generated every 4 switching cycles, this is a value that will determinate how often the control loop is executed and will influence in a great maner the CPU usage and the regulation speed.

ADC configuration

It is very important to synchronize the ADC conversions with the switching frequency to ensure that conversions do not happen while the mosfet is switching, that will minimize the possible noise couple on the target signal.

There are three signals to be converter:

- Input voltage
- Output voltage
- Inductance current

The trigger for the conversion is done by a zero match of the CCU40 as shown in Figure 19.

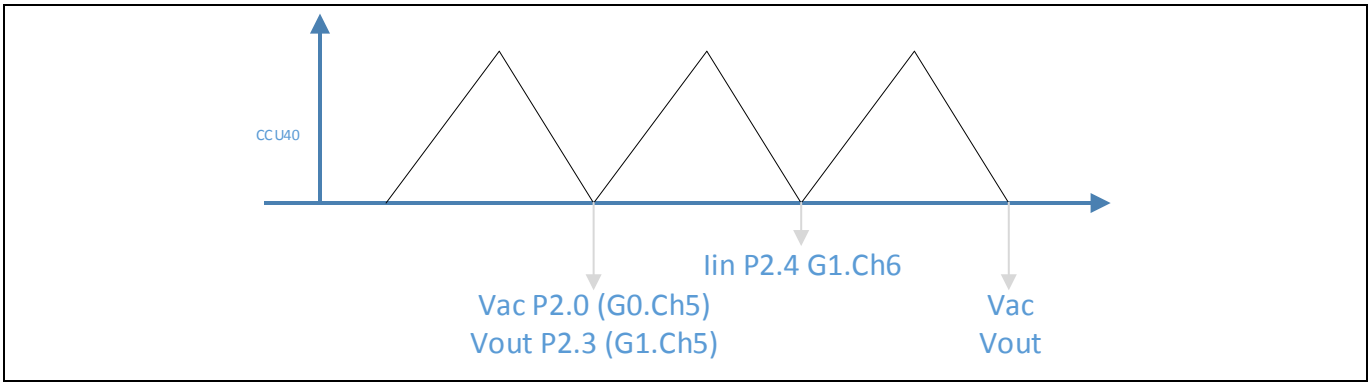

Figure 19 ADC configuration

The protections using comparatos, the PWM generation and ADC conversions are handle in the peripherals automonously without intervention of the CPU.

Another important HW configuration is the CPU and peripheral clock, in the implementation the CPU clock is running at 32MHz while the peripheral clock runs at 64MHz which allows good resolution for the PWM.

3.3 PFC state machine

The PFC track its status with a state machine, the initial staus is “IDLE”.

Upon a call to the SW API PFC_Start() the status changes to “Start request”, as soon as the voltage is over the brown in threshold the status changes to “soft start” and the gate driver starts sending pulses to bring the output voltage to its target, during this time an extra current is required to charge the output capacitor.

Once the output voltage reference reaches its target the status is changed to “tracking”.

The status may change to IDLE by calling the API PFC_Stop(idle) in case it needs to be switch off by SW. Any protection feature will stop the PFC and change its status to the detected failure to report the error.

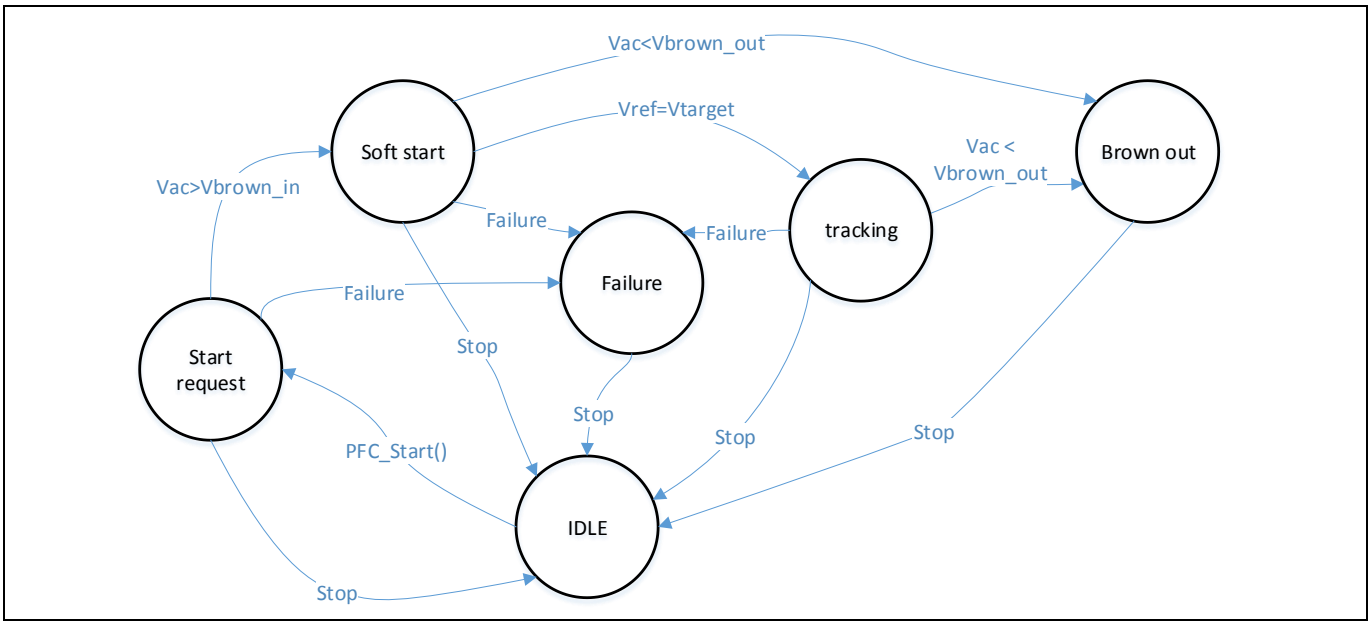

Figure 20 PFC state machine

3.4 Interrupt usage and tasks distribution

There are several different tasks which need to be carried out, all of them related to PFC regulation algorithms, limits and protections which are part of the module layer, most of them need to be executed in regular basics, and those are:

- @ 32KHz
  - Current loop
- @ 4KHz
  - Voltage loop
  - Psuedo PLL
  - Update DCM base duty cycle 1
  - Notch filter
  - Non lineal gain for voltage loop
  - Protections flags checks and other functionality
  - Update DCM base duty cycle 2

There is a single interrupt which handles all the tasks described above, such interrupt is trigger every fouth switching cycle, that means at 32KHz. The current loop is executed every time the interrupt is trigger, the rest of the tasks are executed one out of eight times we enter the interrupt, meaning with 4KHz frequency.

Slot seven is not used.

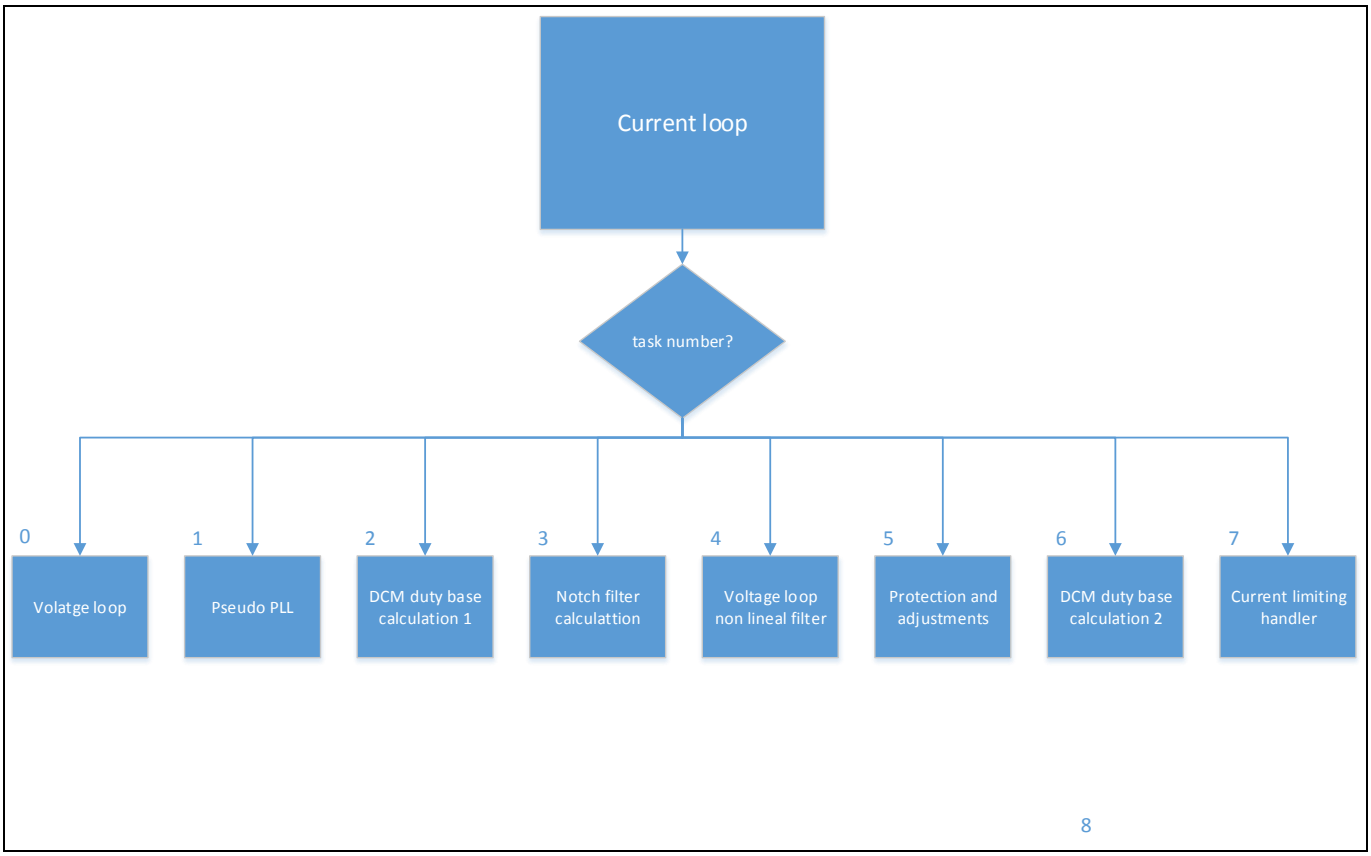

Figure 21 SW tasks distribution

This kind of tasks distribution will ensure a synchronized and time controlled response together with an even distribution of the CPU load.

3.4.1 Current loop

The function of the current loop is to ensure that input current follows the reference given by the voltage loop. It is only executed when the PFC status is tracking or soft start. Inside the control loop a software check for the current protection is done. During the start phase a special case can happen, the input voltage can be bigger than output voltage due to the diode drop (ie. At the peak of the sine wave), during such time a minimum duty cycle is applied until the output voltage is pump up.

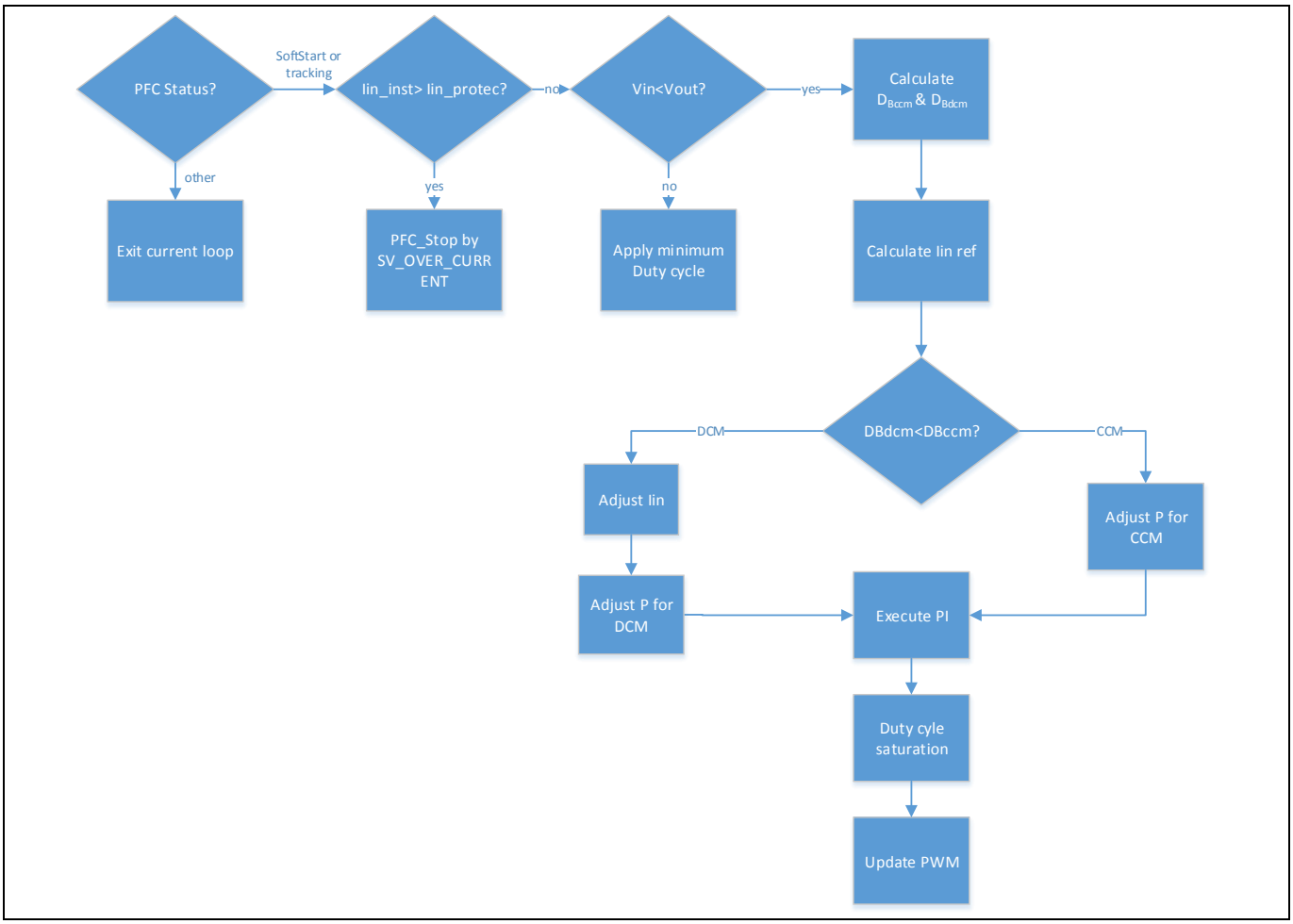

Figure 22 Current loop block diagram

3.4.2 Voltage loop

The voltage loop will take care to set the required instantaneous current as a reference for the current loop.

Due to the fact that the output capacitor value use to be high for keeping low ripple and hold time the nature of the voltage loop in a PFC is slow, therefore the execution frequency of the control loop is choosen to be 4KHz.

Special care has to be taken during start up to allow a smooth voltage ramp the reference is incremented slowly from the current value of the output voltage at the time the request to start is done until the desired output voltage target.

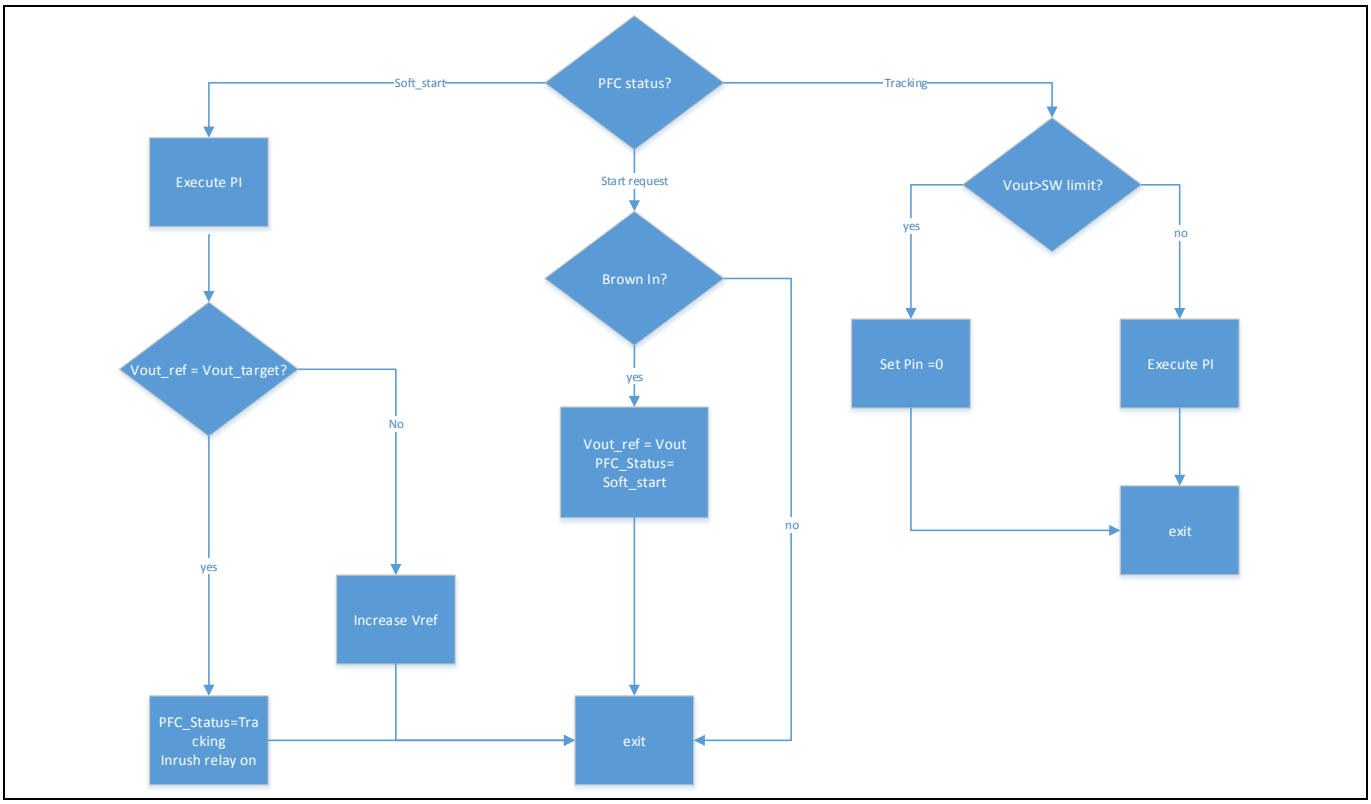

Figure 23 Voltage loop block diagram

3.4.3 Pseudo PLL

The pseudo PLL implements a detection of the zero voltage crossing at the input voltage in SW, since XMC only sees a rectifed value of Vac, we need to detect when the voltage is at its lower value.

To carry out such task, 3 values of the input voltage are kept. A zero crossing is detected when the middle sample is lower than the adjacents and below a give value (in our case 25V) which depends on the sampling frequency and maximum Vac rms.

Every time a crossing is detected the average value of the input voltage and its frequency are calculated, the RMS is extracted by multiplying the average value by a factor (RMS value/average value ~ 1.11).

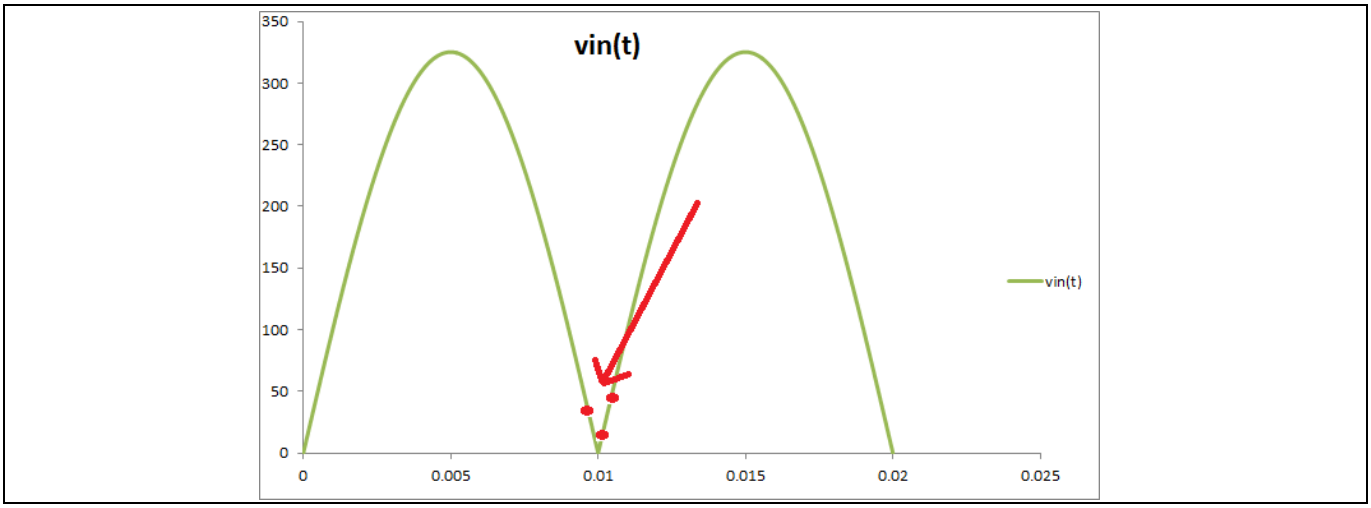

Figure 24 Rectified AC wave

3.4.4 Voltage loop non lineal gain

The non lineal filter just increases the proportional part of the PI voltage loop regulator linearly when the output voltage exit certain value.

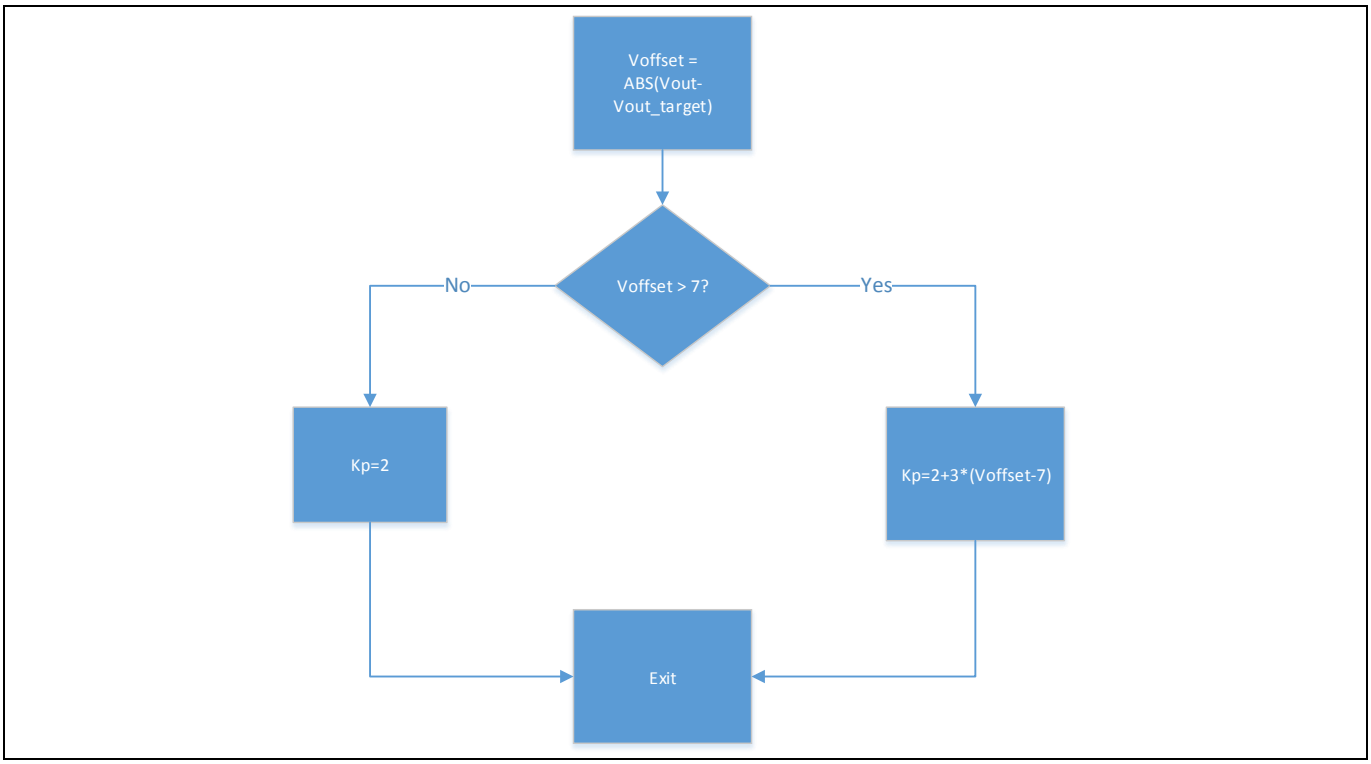

Figure 25 Non lineal gain for output voltage

3.4.5 Protections and adjustments

Critical protections are detected by HW and gate drive is switched off (output OVP and inductance OCP), if a HW protection happens a flag is raised to inform the SW.

SW checks regularly (task 6 in Figure 21) if any SW protection has occurred or if any flag from HW protections is active triggering if required a PFC switch off and changing the status accordingly.

In this section the next protections are cheched:

- HW:
  - Output OVP
  - Inductor OCP
- SW:
  - Overtemperature pin
  - Brown out
  - SW output OVP (average voltage over given threshold)
  - SW overload (output voltage average below given threshold)

In this section an adjustment of the PI current loop gain used in CCM is done to correct the dependency with the output voltage to compensate for the plant variations, equation [10].

3.5 Software header file

One of the major reasons to use a digital controller for power conversion applications is not only because it allows easy integration of communications but as well because the software can be adapted and customized to specific HW.

In this SW example we try to keep a generic approach without fine tunning of specific points to enable an easy porting of the code to a new system.

Nevertheless certain values need to be change depending of the HW.

The Header file is split in the next sections:

- HW parameters
- PFC parameters
- Limits and protections
- Correction factors
- Others

3.5.1 HW paramters

Here we have:

- Input voltage divider: AC input voltage divider ratio
- Output voltage divider: Output voltage divider ratio
- Input current divider: Input current to voltage ratio
- Inductance @ 0A: inductance value in µH @ 0A
- Inductance derating: represent the inductance value decrease with current in µH/A
- Mosfet Cco(tr): approximate mosfet Cco(tr) value in pF (this value can be adjusted to increase Ithd performance)

3.5.2 PFC parameters

In this section we have:

- PFC switching frequency
- Brown In
- Brown Out
- Target output voltage
- InRush relay switch on delay: in number of cycles from first gate pulse
- Output voltage ramp up slope in V/s
- Voltage loop regulator parameters:
    - Kp in Watts/V
    - Ki in Watts/(V*s)
    - Non lineal filter threshold offset
    - Non lineal filter Kp factor
    - VOUT_OFFSET_MAX: limit the maximum Kp used
- Noth filter enable/dissable switch
- Current loop Kp factor
- Current loop Ki
- Input RMS voltage sample average: useful adjust reaction time to brown out

3.5.3 Limits and protections

Here we have:

- SW input current protection
- SW input current limit
- SW_IIN_RMS_LIMIT
- SW output voltage limit
- SW ouput voltage OVP
- SW input conductance limit
- SW overload voltage threshold
- SW current protection @ startup
- SW power limit
- Maximum Soft Start time
- Maximum delta duty cycle
- Maximum duty cycle
- Minimum duty cycle

3.5.4 Correction factors

Several system offset can be adjusted here.

- Input current sense offset: partially correct current sense offset due to filtering
- GD ON_OFF delay correction: correct delays in the gate driver
- Duty base correction factor
- Brown In correction: may correct HW imprecisions
- Duty cycle delta DCM/CCM gain: apply CCM compensator gain when D_{Bccm} < (D_{Bdcm} + this value) to ensure that DCM gain is not applied while CCM mode occurs

3.6 Guide to adapt the SW to a new design

Adapting the SW to a new board requires changes on the header file, apart of the HW resources assignment in case different pins are used. In this section we will have a look to some points that may need special care when modifying the header file.

A set of parameter that needs to be adapted in any case are those related to the board: HW parameters.

From the HW parameters there is one which needs to be trimmed for Ithd improvement at high input current values: MOSFET_CO_TR_pF, its value is highly link with the mosfet output capacitance time related, this value will help to improve Ithd at zero crossing as explain in 2.2.2.

PFC_INDUCTANCE_DERATING_uH_A could be increased if oscillations are observed at the top of the sine wave; this will decrease the compensator gain with increasing current values.

Another important factor to avoid DCM operation while system is in CCM is DUTY_BASE_CORR_FACTOR; such factor as well ensures the right duty cycle base for CCM, (theoretically 1). Such factor defines the threshold used by the SW to apply DCM duty base and the change of gain for the compensator propotional part.

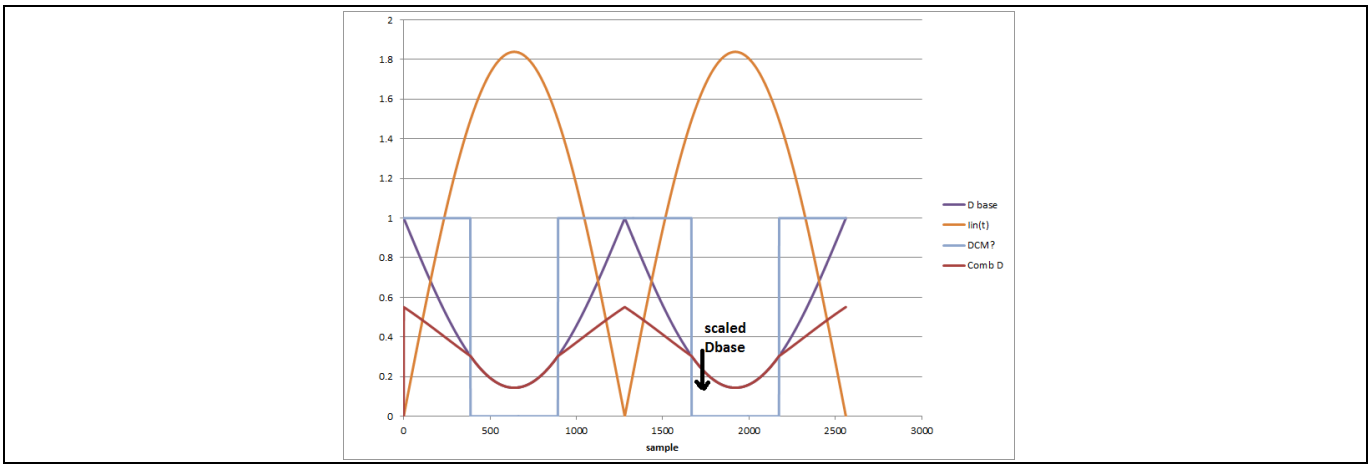

Figure 26 Duty base correction factor effect

By decreasing the correction factor, the crossing point between DCM and CCM will be closer to the 0 crossings and so enlarging a bit the CCM duty cycle base and gain.

The last parameter that we should take care to ensure a that the DCM gain of the compensator is not using during CCM operation is: DCYCLE_DELTA_CCM_DCM_GAIN, as explain in Figure 11, if oscilations are observed during the transition from DCM to CCM this parameters should be increase or the inductance value should be corrected.

Overall parameters to trim the current loop PI are:

CURRENT_LOOP_Kp_FACTOR_CCM: defines the gain factor for CCM operation mode

CURRENT_LOOP_Kp_FACTOR_DCM: defines the gain factor for DCM operation mode (only integer values are allowed)

CURRENT_LOOP_Ki: integrative part for the current loop

V_LIMIT_I_PI_GAIN: this value limits the maximum gain of the compensator during DCM by adding a constant value to Vin in formula [11].

The Brown out reaction time and filtering of possible voltage drops can be adjusted with the number of samples used in the cumulative moving average filter for Vin RMS: VIN_RMS_AVG_FACTOR, the bigger the factor the slower the reaction time will be.

The variables N_CYCLES_SKIP_ILOOP will determine how many switching cycles there will be between the update of the current loop, executing the current loop too often may lead to saturation of the CPU, 32KHz update rate is adviced.

4 Resource Listing

- **Link to Infineon PFC_CCM_800W Application Kit**

Attention: Revision History

Major changes since the last revision

Page or Reference	Description of change
0.1	Draft version, prerelease

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